

**REMARKS**

Claims 1 and 20-34 are pending. Claims 20-34 have been added to round out the scope of the invention. Applicants reserve the right to pursue the original claims and other claims in this and in other applications.

The specification stands objected to because of informalities regarding the designation of the application and cross reference to the parent application. The specification has been amended according to the Examiner's instructions. No new matter has been entered. Withdrawal of the objection is respectfully requested.

Claim 1 stands rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of U.S. Patent No. 6,717,853. Claim 1 of the instant application has been amended. Claim 1 recites, *inter alia*, "a plurality of array ground lines" and "a plurality of flash memory transistors each having a respective source, drain, and control gate, each source being connected to a respective one of said plurality of array ground lines, each drain being coupled to said bit line, and each control gate being coupled to said word line" which is not cited in U.S. Patent No. 6,717,853. Therefore, there cannot be double patenting under 35 U.S.C. 101. Withdrawal of the rejection is respectfully requested.

Application No.: 10/758,103

Docket No.: M4065.0546/P546-A

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By 

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